AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): An integrated circuit package comprising:

a) a plurality of leads each having a first face and a second face opposite to said first face;

b) a die pad having a first face and a second face opposite to said first face, wherein said second face of said die pad is orthogonally offset from said second face of said leads, such that said second face of said die pad and said second face of said leads are not coplanar;

c) an integrated circuit chip substantially laterally disposed between said plurality of leads and having a first face and a second face opposite to said first face, whereby said first face of said integrated circuit chip is proximate to said second face of said die pad and is coupled to said second face of said die pad; and

d) a plurality of wires linking said plurality of leads to said integrated circuit chip, each of said plurality of wires comprising:

a first end electrically conductively joined to said first face of said IC chip, wherein said first end is disposed between a first plane defined by said second face of said die pad and a second plane defined by said first face of said integrated circuit chip, and

a second end electrically conductively joined to said first face of one of said plurality of leads, wherein said second end is disposed between a third plane defined by said first face of said die pad and a fourth plane defined by said first face of one of said plurality of leads, and

wherein the area of said first face of said die pad in said third plane is larger than the area of said second face in said first plane.

2. (withdrawn): The integrated circuit package according to claim 1, wherein said first face of said die pad is adapted to direct coupling with a thermal dissipation element.

3. (withdrawn): The integrated circuit package according to claim 1, further comprising:

e) an encapsulant surrounding said first face of said integrated circuit chip, said first faces of said plurality of leads, said wires, and said second face of said die pad, and wherein said first face of said die pad is adapted to direct coupling with a thermal dissipation element.

4. (withdrawn): The integrated circuit package according to claim 3, wherein said encapsulant is a polymer-based molding compound.

5. (withdrawn): The integrated circuit package according to claim 3, wherein a planar surface is formed comprising said first face of said die pad and an outer surface of said encapsulant.

6. (original): The integrated circuit package according to claim 1, wherein said plurality of leads and said die pad are composed of a common copper alloy.

7. (original): The integrated circuit package according to claim 1, wherein said plurality of wires are composed of one of a group comprising: gold, gold with some level of impurities, aluminum, and copper.

8. (withdrawn): The integrated circuit package according to claim 1, further comprising:

e) a thermal dissipation element having a first face and a second face opposite to said first face, wherein said second face of said thermal dissipation element is coupled to said first face of said die pad.

9. (withdrawn): The integrated circuit package according to claim 8, wherein said thermal dissipation element comprises a heat sink for a single integrated circuit chip.

10. (withdrawn): The integrated circuit package according to claim 8, wherein said thermal dissipation element comprises a heat sink for a plurality of integrated circuit chips.

11. (withdrawn): The integrated circuit package according to claim 1, wherein:

said second face of said die pad comprises:

an inner surface,

a peripheral surface, and

an edge defining the boundary between said inner surface and said peripheral surface; and

wherein the space between said inner surface and said first face is greater than the space between said peripheral surface and said first face, such that said inner portion is offset from said peripheral portion.

12. (withdrawn): The integrated circuit according to claim 1, wherein said second face of said die pad comprises:

an inner surface,

a peripheral surface, and

a reservoir defining the boundary between said inner surface and said peripheral surface.

13. (original): The integrated circuit package according to claim 1, wherein:

said plurality of leads and said die pad are formed from a leadframe, said leadframe comprising:

an outer frame supporting said plurality of leads extending substantially inward from said outer frame, and

a plurality of tie bars securing said outer frame to said die pad, substantially centrally disposed within said outer frame; and

wherein each of said plurality of tie bars includes a mechanical depression, such that an offset is created between said die pad and said plurality of leads.

14. (currently amended): An integrated circuit package according to claim 1, further comprising:

~~a) a plurality of leads each having a first face and a second face opposite to said first face;~~

~~b) a die pad having a first face and a second face opposite to said first face, wherein said second face of said die pad is orthogonally offset from said second face of said leads, such that said second face of said die pad and said second face of said leads are not coplanar;~~

~~c) an integrated circuit chip substantially laterally disposed between said plurality of leads and having a first face and a second face opposite to said first face, whereby said first face of said integrated circuit chip is proximate to said second face of said die pad and is coupled to said second face of said die pad;~~

~~d) a plurality of wires linking said plurality of leads to said integrated circuit chip, each comprising:~~

~~a first end electrically conductively joined to said first face of said integrated circuit chip, and~~

~~a second end electrically conductively joined to said first face of one of said plurality of leads;~~

e) an annular element substantially laterally disposed between said integrated circuit chip and said plurality of leads such that said annular element substantially encircles said integrated circuit chip; and

f) at least one secondary wire linking said integrated circuit chip to said annular element, each wire having:

a first end electrically conductively joined to said first face of said integrated circuit chip, and

a second end electrically conductively joined to said first face of said annular element.

15. (withdrawn): The integrated circuit package according to claim 14, wherein said annular element is electrically grounded.

16. (withdrawn): The integrated circuit package according to claim 14, wherein said annular element comprises a power source.

17. (withdrawn): The integrated circuit package according to claim 14, wherein said annular element is circular.

18. (withdrawn): The integrated circuit package according to claim 14, wherein said annular element is elliptical.

19. (withdrawn): The integrated circuit package according to claim 14, wherein said annular element is a polygon.

20. (currently amended): An integrated circuit package according to claim 1, further comprising:

~~a) a plurality of leads each having a first face and a second face opposite to said first face;~~

b) ~~an integrated circuit chip substantially laterally disposed between said plurality of leads, and having a first face and a second face opposite to said first face~~;

c) a thermal dissipation element having a first face and a second face opposite to said first face,

wherein said second face of said thermal dissipation element is proximate to said first face of said ~~integrated circuit chip~~ die pad and is coupled to said first face of said ~~integrated circuit chip~~ die pad through a first coupling material, and

wherein said second face of said thermal dissipation element extends laterally such that it overhangs said first face of each of said plurality of leads; and

d) a plurality of wires linking said plurality of leads to said integrated circuit chip, each wire comprising:

a first end electrically conductively joined to said first face of said integrated circuit chip, wherein said first end is disposed between said second face of said thermal dissipation element and said first face of said integrated circuit chip, and

a second end electrically conductively joined to said first face of one of said plurality of leads, wherein said second end is disposed between said second face of said thermal dissipation element and said first face of said one of said plurality of leads.

21. (withdrawn): The integrated circuit package according to claim 20, wherein said thermal dissipation element comprises a heat sink.

22. (withdrawn): The integrated circuit package according to claim 20, wherein said second face of said thermal dissipation element is further coupled to said first face of each of said plurality of leads through a second coupling material.

23. (withdrawn): The integrated circuit package according to claim 22, wherein said second coupling material is electrically non-conductive.

24. (withdrawn): The integrated circuit package according to claim 22, wherein said second coupling material is thermally conductive.

25. (withdrawn): The integrated circuit chip according to claim 14, wherein:

said plurality of leads, said die pad, and said annular element are formed from a leadframe, said leadframe comprising:

an outer frame supporting said plurality of leads extending substantially inward from said outer frame,

said die pad, substantially centrally disposed within said outer frame,

said annular element, substantially laterally disposed between said die pad and said outer frame, such that said annular element substantially encircles said die pad, and

a plurality of tie bars securing said outer frame to said annular element and securing said annular element to said die pad; and

each of said plurality of tie bars includes a mechanical depression, such that an offset is created between said die pad and said annular element..